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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

WANG, ALBERT C

ART UNIT	PAPER NUMBER
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2115

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/601,375

Applicant(s)

HILGENDORF ET AL

Examiner

Albert Wang

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 February 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This Office action is responsive to the amendment filed 13 February 2006.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi, U.S. Patent No. 7,000,130, in view of Santhanam et al., U.S. Patent No. 6,971,038 ("Santhanam").

As per claim 1, Adachi teaches a processing system, comprising:

a processor comprising logic coupled to receive a clock signal via a plurality of local clock buffers, wherein the processor is configured to operate in a first power mode and a second power mode, and wherein the processor dissipates different amounts of electrical power in the first and second power modes (fig. 3, comprising functional blocks 205 and 207);

a pulse train generator configured to produce three or more pulse trains, wherein each of the three or more pulse trains corresponds to a different level of electrical power dissipation within the processor (fig. 5, LFSR 510; col. 1, lines 15-25; col. 7, lines 10-30, logical one, logical zero, and output of prior stage);

selection logic coupled to receive each of the pulse trains produced by the pulse train generator and configured to produce a selected one of the pulse trains (fig. 5, multiplexor of stage 512N);

control logic coupled to the selection logic and configured to control the selection logic to effect transitions between the first and second power modes wherein during each transition between the first and second power modes the selection logic produces at least three of the three or more pulse trains produced by the pulse train generator in sequence such that the electrical power dissipation of the processor changes monotonically during the transition (col. 4, line 61 – col. 5, line 6; col. 7, line 64 – col. 8, line 9); and

a timed clock control distribution network coupled to receive the clock signal masked by the sequence of pulse trains produced by the selection logic and configured to provide the clock signal to the local clock buffers such that each of the local clock buffers receives the clock signal at the same time (fig. 3, TCLK 307 provided to buffers 325 and 327; col. 3, line 56 – col. 4, line 25).

However, Adachi does not expressly teach providing the sequence of pulse trains to each of a plurality of local clock buffers. Santhanam teaches a local clock tree whose structure may be adapted to distribute the sequence of pulse trains (fig. 2). Instead of masking the global clock at gate 50, the global clock may be masked at local clock buffers 52, if the sequence of pulse trains were distributed to the enable inputs of the clock buffers. At the time of the invention, it would have been obvious to one of ordinary skill in the art that the structure of Santhanam's local clock tree to may be adapted distribute Adachi's sequence of pulse trains to a plurality of local clock buffers, as masking the clock signal before distributing is equivalent to masking the distributed clock signal at the local clock buffers.

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As per claim 2, since power dissipation is a direct function of clock frequency, the first power mode then arbitrarily is at higher frequency, or the frequency of the free-running clock.

As per claim 3, Adachi teaches the three or more pulse trains comprises: a constant high pulse train having a constant high level, a constant low pulse train having a constant low voltage level, and one or more pulse trains that alternate between the constant high voltage level and the constant low voltage level (col. 7, lines 10-30);

As per claim 4, since Adachi teaches logic gate 306 is an AND gate formed out of a NAND gate and an inverter (col. 3, lines 65-66), it is obvious that using a NAND gate for logic gate 306 would invert the logic, so that when the processor is operates in the first power mode, the selection logic produces the first constant pulse train, and when the processor is operating in the second power mode the selection logic produces the second constant pulse train.

As per claims 5-7, Adachi teaches both increasing and decreasing power dissipation monotonically (col. 4, line 61 – col. 5, line 6).

As per claim 8, local clock buffers such as those in Santhanam (fig. 2) would mask the clock signal dependent on the sequence of pulse trains.

As per claim 9, Adachi teaches the control logic comprises a state machine ramp control system and a delay counter coupled to the state machine ramp control system (fig. 5, col. 7, line 64 – col. 8, line 9).

As per claim 10, Adachi teaches the state machine ramp is configured to cycle and reset the delay counter, and wherein the delay counter comprises a plurality of programmable storage elements (fig. 5, col. 7, line 64 – col. 8, line 9).

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As per claim 28, local clock buffers such as those in Santhanam (fig. 2, clock buffers 52) is coupled to receive the clock signal and the sequence of pulse trains from the timed clock control distribution network, and configured to provide the clock signal to the logic of the processor dependent upon the sequence of pulse trains.

As per claim 11, Adachi teaches in a processing system comprising a processor coupled to receive a clock signal and configured to operate in a first power mode and a second power mode, a method for transitioning between the first and second power modes, the method comprising:

producing three or more pulse trains each corresponding to a different level of electrical power dissipation within the processor (fig. 5, with LSFR 510; col. 1, lines 15-25; col. 7, lines 10-30, logical one, logical zero, and output of prior stage);

during a transition between the first and second power modes, producing at least three of the three or more pulse trains in sequence such that the electrical power dissipation of the processor changes monotonically during the transition (col. 4, line 61 – col. 5, line 6); and

providing the clock signal dependent upon the sequence of pulse trains to each of a plurality of local clock buffers such that each of the local clock buffers receives the clock signal at the same time, wherein each of the local clock buffers is coupled to receive the clock signal and the sequence of pulse trains, and configured to provide the clock signal to the processor (fig. 3, TCLK 307 provided to buffers 325 and 327; col. 3, line 56 – col. 4, line 25).

However, Adachi does not expressly teach providing the sequence of pulse trains to each of a plurality of local clock buffers. Santhanam teaches a local clock tree whose structure may be adapted to distribute the sequence of pulse trains (fig. 2). Instead of masking the global clock at gate 50, the global clock may be masked at local clock buffers 52, if the sequence of pulse trains were distributed to the enable inputs of the clock buffers. At the time of the invention, it would have been obvious to one of ordinary skill in the art that the structure of Santhanam's local clock tree to may be adapted distribute Adachi's sequence of pulse trains to a plurality of local clock buffers, as masking the clock signal before distributing is equivalent to masking the distributed clock signal at the local clock buffers.

As per claim 12, Adachi teaches the three or more pulse trains comprises: a constant high pulse train having a constant high level, a constant low pulse train having a constant low voltage level, and one or more pulse trains that alternate between the constant high voltage level and the constant low voltage level (col. 7, lines 10-30);

As per claim 13, Adachi teaches during a transition between the first and second power modes, producing a first constant level pulse train. at least one of the one or more pulse trains that alternate between the constant voltage level and the constant low voltage level. and a second constant level pulse train in sequence such that the electrical power dissipation of the processor changes monotonically during the transition (col. 4, line 61 – col. 5, line 6).

As per claim 22, Adachi teaches a processing system, comprising:

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a processor comprising logic coupled to receive a clock signal via a plurality of local clock buffers, wherein the processor is configured to operate in a first power mode and a second power mode, and wherein the processor dissipates different amounts of electrical power in the first and second power modes (fig. 3, comprising functional blocks 205 and 207);

a pulse train generator configured to produce three or more pulse trains comprising: a first constant pulse train having a constant first voltage level, a second constant pulse train having a constant second voltage level, and one or more pulse trains that alternate between the first and second voltage levels, wherein each of the three or more pulse trains corresponds to a different level of electrical power dissipation within the processor (fig. 5, LFSR 510; col. 1, lines 15-25; col. 7, lines 10-30, logical one, logical zero, and output of prior stage);

selection logic coupled to receive each of the pulse trains produced by the pulse train generator and configured to produce a selected one of the pulse trains (fig. 5, multiplexor of stage 512N);

control logic coupled to the selection logic and configured to control the selection logic to effect transitions between the first and second power modes, wherein during each transition between the first and second power modes the selection logic produces at least three of the three or more pulse trains produced by the pulse train generator in sequence such that the electrical power dissipation of the processor changes monotonically during the transition (col. 4, line 61 – col. 5, line 6; col. 7, line 64 – col. 8, line 9); and

a timed clock control distribution network coupled to receive the clock signal masked by the sequence of pulse trains produced by the selection logic and configured to provide the clock signal to the local clock buffers such that each of the local clock buffers receives the clock signal at the same time (fig. 3, TCLK 307 provided to buffers 325 and 327; col. 3, line 56 – col. 4, line 25).

However, Adachi does not expressly teach providing the sequence of pulse trains to each of a plurality of local clock buffers. Santhanam teaches a local clock tree whose structure may be adapted to distribute the sequence of pulse trains (fig. 2). Instead of masking the global clock at gate 50, the global clock may be masked at local clock buffers 52, if the sequence of pulse trains were distributed to the enable inputs of the clock buffers. At the time of the invention, it would have been obvious to one of ordinary skill in the art that the structure of Santhanam's local clock tree to may be adapted distribute Adachi's sequence of pulse trains to a plurality of local clock buffers, as masking the clock signal before distributing is equivalent to masking the distributed clock signal at the local clock buffers.

As per claim 23, since power dissipation is a direct function of clock frequency, the first power mode then arbitrarily is at higher frequency, or the frequency of the free-running clock.

As per claim 24, since Adachi teaches logic gate 306 is an AND gate formed out of a NAND gate and an inverter (col. 3, lines 65-66), it is obvious that using a NAND gate for logic gate 306 would invert the logic, so that when the processor is operates in the first power mode, the selection logic produces the first constant pulse train, and when the

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processor is operating in the second power mode the selection logic produces the second constant pulse train.

As per claims 25 and 26, Adachi teaches both increasing and decreasing power dissipation monotonically (col. 4, line 61 – col. 5, line 6).

As per claim 27, Adachi teaches the first voltage level is greater than the second voltage level (col. 7, lines 10-30).

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PRIMARY EXAMINER